

Dual N-Channel 2.5-V (G-S) MOSFET

GENERAL DESCRIPTION

The ME9926 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

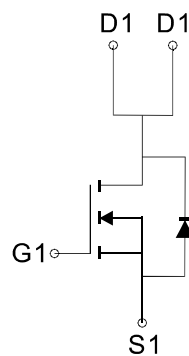
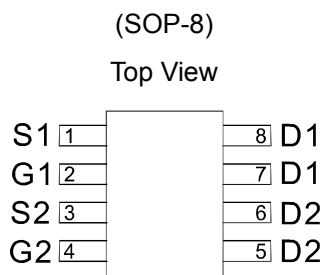
FEATURES

- $R_{DS(ON)} \leq 29m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leq 42m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

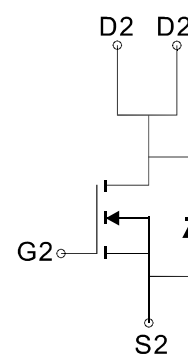
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION



N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Steady State	Unit
Drain-Source Voltage	V_{DSS}	20	V
Gate-Source Voltage	V_{GSS}	± 12	V
Continuous Drain Current	I_D	6	A
Pulsed Drain Current	I_{DM}	28	A
Maximum Power Dissipation	P_D	$T_A=25^\circ C$	2.0
		$T_A=70^\circ C$	1.2
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	$T \leq 10 \text{ sec}$	62.5
		Steady State	88
Thermal Resistance-Junction to Case	$R_{\theta JC}$	50	$^\circ C/W$

* The device mounted on 1in² FR4 board with 2 oz copper

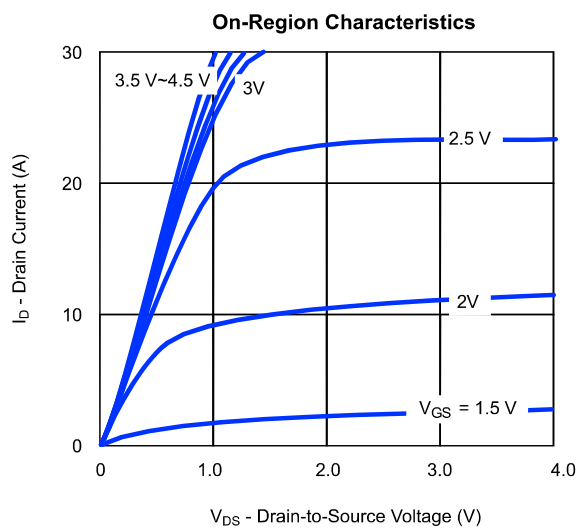
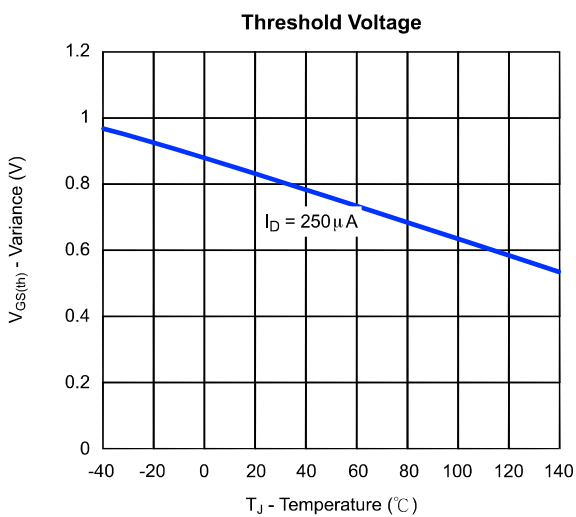
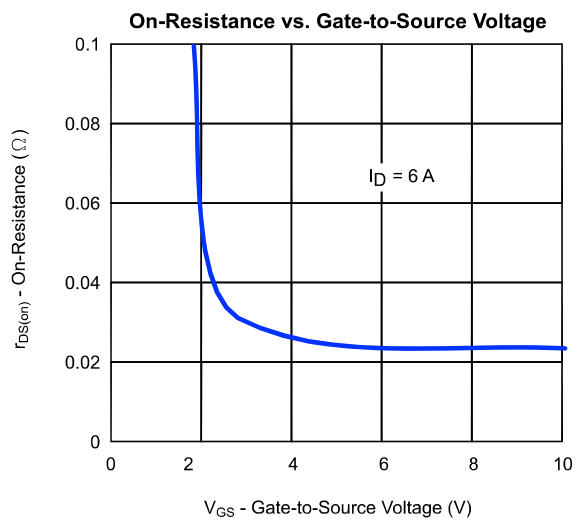
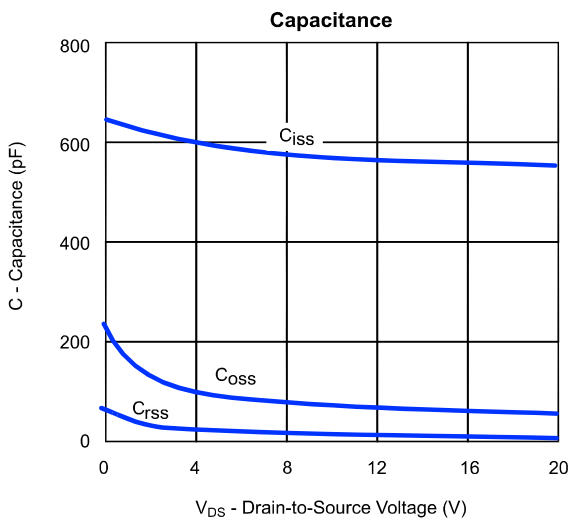
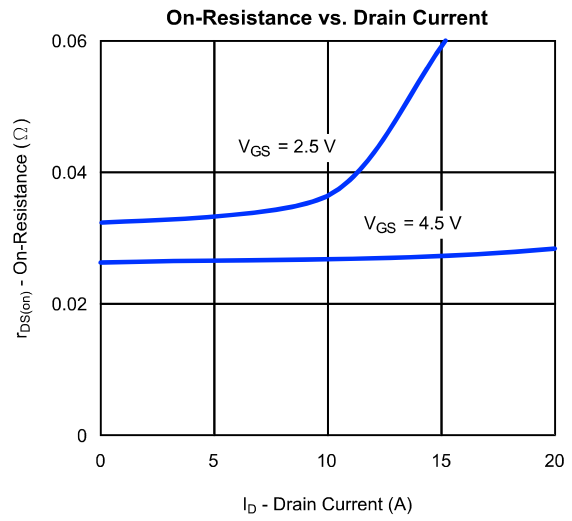
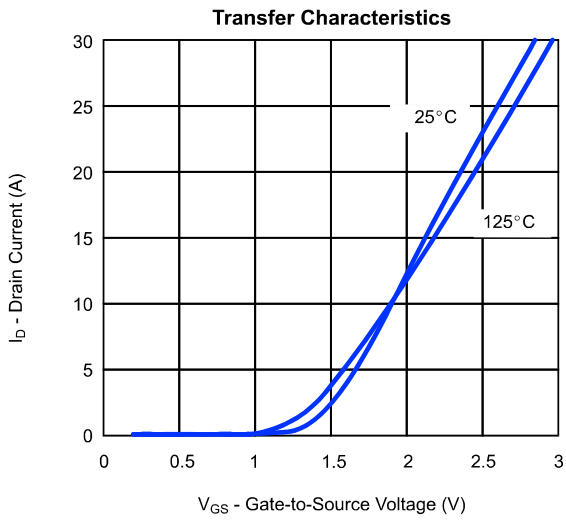
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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

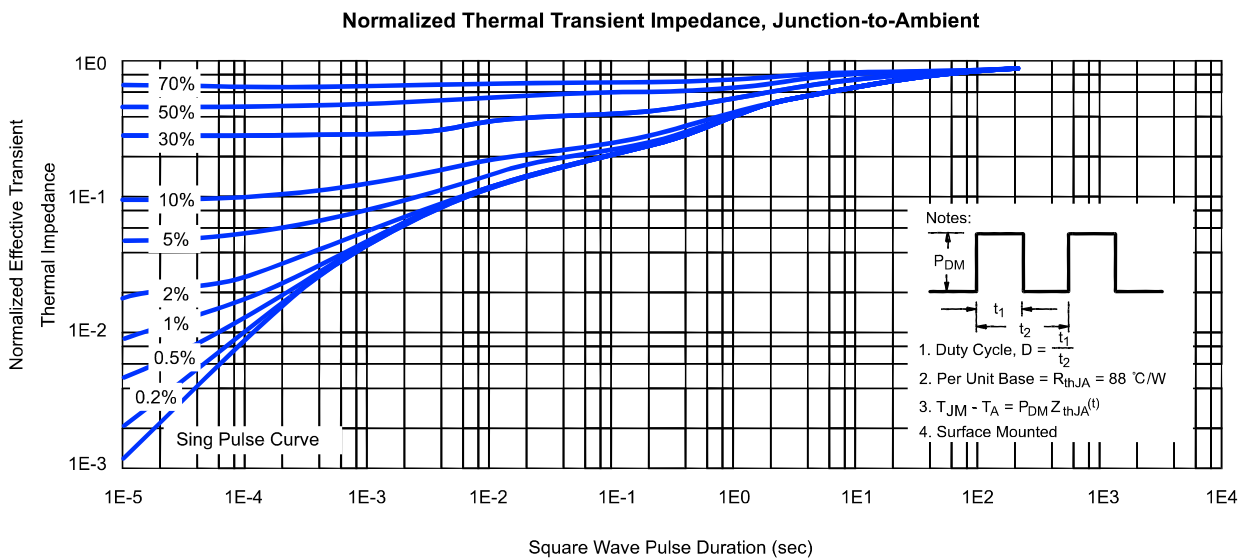
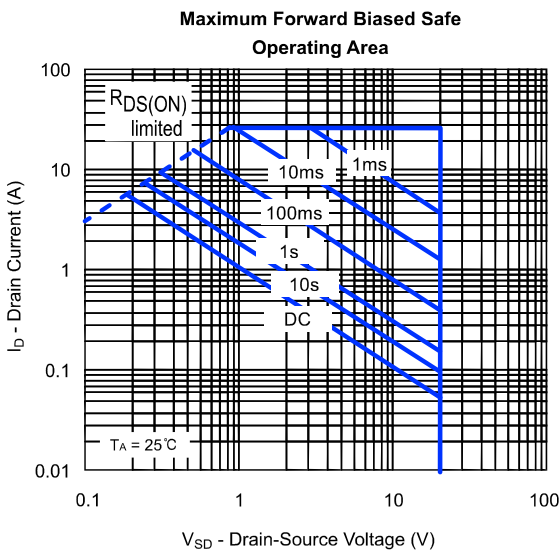
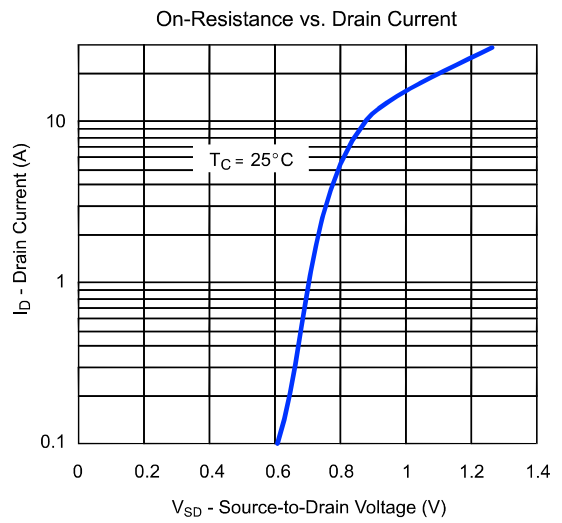
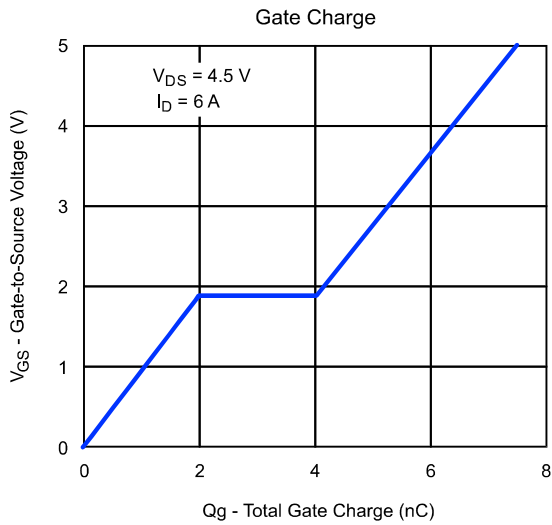
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0, I _D =250 μA	20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	0.4		0.9	V
I _{GSS}	Gate Body Leakage	V _{DS} =0V, V _{GS} =±12V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	μA
I _{D(ON)}	On-State Drain Current ^a	V _{DS} ≥ 5V, V _{GS} = 4.5V	30			A
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =4.5V, I _D = 6.0A		22	29	mΩ
		V _{GS} =2.5V, I _D = 5.2A		32	42	
V _{SD}	Diode Forward Voltage	I _S =1.7A, V _{GS} =0V		0.74	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =10V, V _{GS} =4.5V, I _D =6.0A		9.5		nC
Q _{gs}	Gate-Source Charge			2.1		
Q _{gd}	Gate-Drain Charge			2.6		
R _g	Gate resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		0.8		Ω
t _{d(on)}	Turn-On Delay Time	V _{DD} =10V, I _D =1.0A, V _{GEN} =4.5V R _G =6Ω		9.5		ns
t _r	Turn-On Rise Time			22		
t _{d(off)}	Turn-Off Delay Time			47		
t _f	Turn-Off Fall Time			2.6		
C _{iss}	Input capacitance	V _{DS} =15V, V _{GS} =0V, f=1.0MHz		550		pF
C _{oss}	Output Capacitance			76		
C _{rss}	Reverse Transfer Capacitance			20		

Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

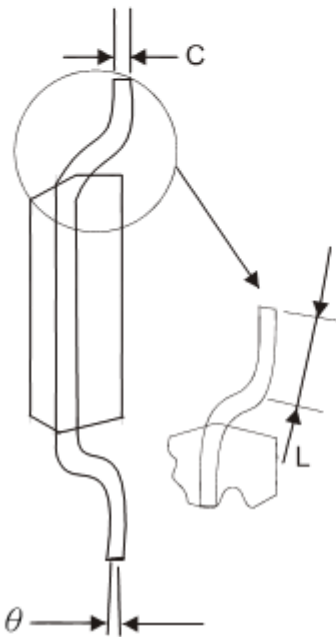
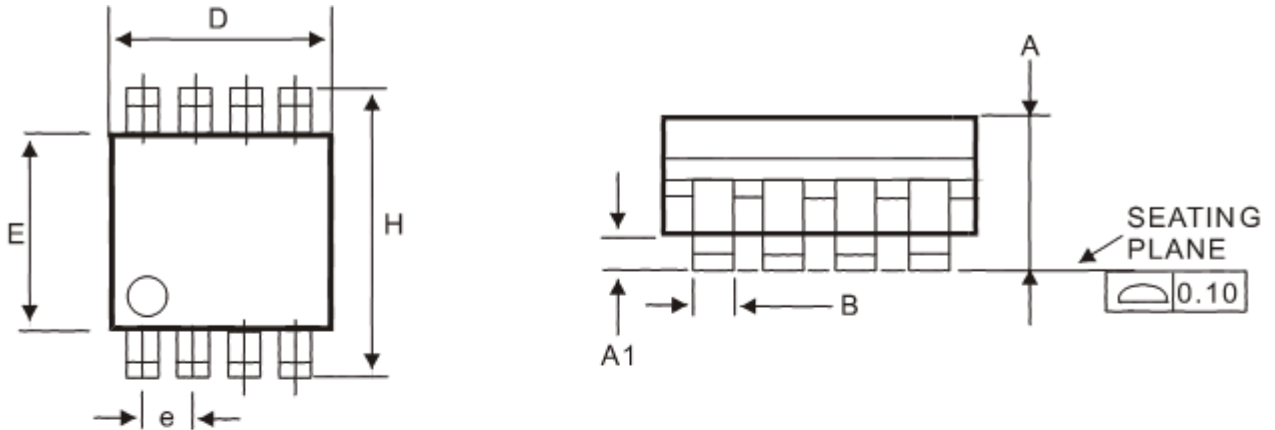
Typical Characteristics (T_J = 25°C Noted)



Typical Characteristics (T_J = 25°C Noted)



SOP-8 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.