Switching Regulators

PRODUCT DESCRIPTION

Application Note 28103.30

Series STR-W6750 Off-Line Quasi-Resonant Switching Regulators

INTRODUCTION

The Series STR-W6750 devices are hybrid integrated circuits (HICs) with a built-in power MOSFET and a control IC designed for quasi-resonant type switch-mode power supplies (SMPS). In normal operation, the HIC provides high efficiency and low EMI noise with bottom-skip quasi-resonant operation during light output loads. Low power consumption is also achieved by blocking (intermittent) oscillation during an auto-burst mode and reduced even further in a manually triggered (clamping an output voltage) standby mode.

The HIC is supplied in a seven-pin fully-molded TO-220-style package with pin 2 deleted, which is suitable for downsizing and standardizing of an SMPS by reducing external component count and simplifying circuit design.

Features

- Blocking (or intermittent) oscillation operation by reducing output voltage in the standby mode.
- In addition to the standard quasi-resonant operation, a bottom-skip function is available for increased efficiency from light to medium load.
- Soft-start operation at start-up.
- Reduced switching noise (compared to conventional PWM hard-switching solution) with a step-drive function.
- Built-in avalanche-energy-guaranteed power MOSFET (to simplify surge-absorption circuit; no V_{DSS} derating is required).
- Overcurrent protection (OCP), overvoltage protection (OVP), overload protection (OLP), and maximum ON-time control circuits are incorporated. → OVP and OLP go into a latched mode.
- Able to save SMPS design time with present designs and evaluation processes.

All performance characteristics given are typical values for circuit or system baseline design only and, unless otherwise stated, are at the nominal operating voltage and an ambient temperature of +25°C, unless otherwise stated.

TERMINAL FUNCTIONS

V_{CC} (Pin 4)

Start-up circuit

The start-up circuit detects the V_{CC} pin voltage (pin 4), and makes the control IC start and stop operation. The power supply of the control IC (V_{CC} pin input) employs a circuit as shown in Figure 1. At start-up, C3 is charged through a start-up resistor R2. The R2 value needs to be set for more than the hold current of the latch circuit (140 µA max.) and to operate at the minimum ac input.

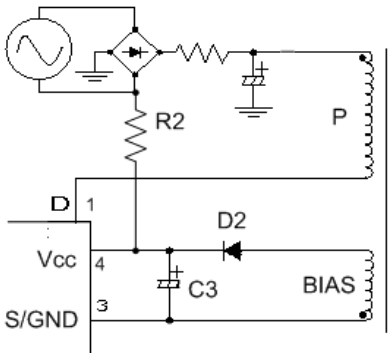

Figure 1 – External start-up circuit

If the value of R2 is too high, the C3 charge current will be reduced. Consequently, it will take longer to reach the operation start-up voltage. The V_{CC} pin voltage falls immediately after the control circuit starts its operation. The voltage drop can be reduced by increasing C3's capacitance. Therefore, to maintain the start-up operation, even if the rise of the bias winding voltage is slow, the V_{CC} pin voltage would not fall to the operation-stop voltage. However, too large a C3 capacitance will cause an improperly long time to reach the operation start after the initial power turn on.

In general, SMPS performs its start-up operation properly with a value of C3 between 4.7 µF and 47 µF, and R2 between 47 kΩ and 150 kΩ for 120 V narrow or universal ac input, and 82 kΩ to 330 kΩ for 200 V narrow ac input.

As shown in Figure 2, the circuit current is limited to 100 µA max (V_{CC} = 15 V, and resistor R2 with appropriate high resistance value for the circuit) until the control circuit starts its operation. Once the V_{CC} pin voltage reaches 18.2 V, the control circuit starts its operation by the start-up circuit, and supply current is increased. Once the V_{CC} pin voltage drops down to lower than the operation-stop voltage 9.7 V, the UVLO circuit operates to stop the control circuit, and the IC returns to its initial state prior to start-up.

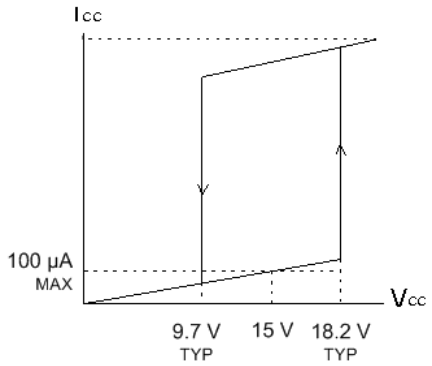

Figure 2 – I_{CC} vs. V_{CC}

Bias/drive winding

After the control circuit starts its operation, the power supply is operated by rectifying and smoothing the voltage of the bias winding. Figure 3 shows the start-up voltage waveform of the V_{CC} pin. The bias winding voltage does not immediately increase up to the set voltage after the control circuit starts its operation. That is why the V_{CC} pin voltage starts dropping. The operation-stop voltage is set as low as 10.6 V (max), the bias winding voltage reaches a stabilized voltage before it drops to the operation-stop voltage, and the control circuit continues its operation. The bias winding voltage, in normal power supply operation, is set for the voltage across C3 to be higher than the operation-stop voltage [$V_{CC(OFF)}$ 10.6 V(max.)] and lower than the OVP-operation voltage [$V_{CC(OVP)}$ 25.5 V(min.)].

In an actual power supply circuit, the Vcc pin voltage might be changed by the value of secondary output current as shown in Figure 4. Because of the low circuit current of the STR-W6750, C3 is fully charged by the surge voltage generated instantly after the MOSFET turns OFF. In order to prevent this, it is effective to add a resistor (R7) of several ohms to tens

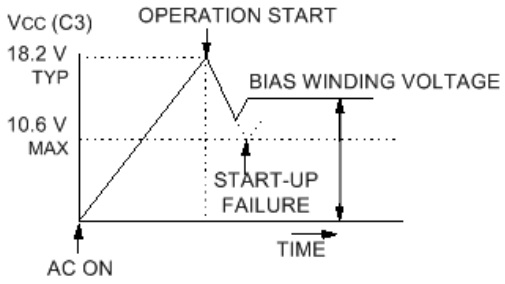

Figure 3 – V_{CC} after start-up

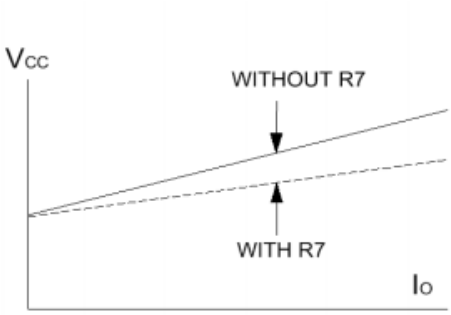

Figure 4 – V_{CC} vs. I_O (secondary load)

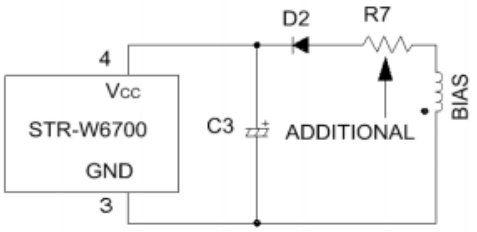

Figure 5 – V_{CC} peripheral circuit with R7

of ohms in series with the diode as shown in Figure 5. The optimum value of the additional resistor is determined in accordance with the specifications of the transformer because the V_{CC} pin voltage is determined by construction of the transformer.

Furthermore, the variation ratio of the V_{CC} pin voltage becomes worse due to a loose coupling between primary and secondary windings of the transformer (the coupling between the bias winding and the stabilized output winding for the constant voltage control). Therefore, when designing a transformer, the winding position of the bias winding needs to be studied carefully.

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036

SanKen

Overvoltage protection (OVP) circuit

If V_{CC}, reference the S/GND pin, exceeds 27.7 V, the OVP circuit of the control IC starts its operation and the fault mode is latched by the latch circuit, the control IC stopping its oscillation. Generally, the V_{CC} pin voltage is supplied from the bias winding of the transformer, and the voltage is in proportion to the output voltage; thus, the OVP circuit also operates in the case of overvoltage output of the secondary side, e.g., when the voltage detection circuit is open.

The secondary output voltage (V_O) for the OVP operation is obtained from the following:

$$V_{O(OVP)} = \frac{V_O \text{ in normal operation}}{V_{CC} \text{ in normal operation}} \times 27.7 \text{ V}$$

Latch circuit

OVP and OLP fault modes latch the oscillation output LOW, which stops the power supply circuit operation. The holding current of the latch circuit is 140 µA (max, T_A = 25°C) when the V_{CC} pin voltage is "Operation-stop voltage – 0.3 V".

In order to prevent malfunction caused by, for instance, noise, a delay time is programmed into a timer circuit, which will prohibit the latch circuit operation until the OVP or OLP circuit keep operating for more than a programmed time. During the latched mode, the regulator circuit (or constant voltage circuit) keeps running, the circuit current being maintained at a high level, and the V_{CC} pin voltage dropping.

When the V_{CC} pin voltage drops down to the operation-stop voltage (9.7 V), the voltage starts rising again as the circuit current becomes less than 140 µA. When the V_{CC} pin voltage reaches the operation-start voltage (18.2 V), the circuit current increases, and the voltage drops again. Consequently, the V_{CC} pin voltage is maintained between 9.7 V and 18.2 V in the latched mode. Figure 6 indicates the voltage waveform in the latched mode. The latched mode is released by decreasing the V_{CC} pin voltage to below 7.2 V, in general, by restarting.

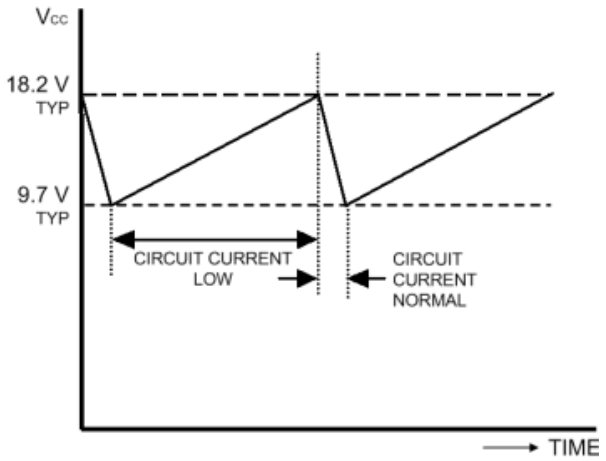

Figure 6 – V_{CC} during latch mode

SS/OLP (Pin 5)

Through the SS/OLP pin, soft-start and overload protection is realized by connecting a 0.47 µF to 3.3 µF capacitor to the pin.

Soft-start operation at start-up of power supply

At the power supply start-up, an external capacitor is charged up to the soft-start operation threshold voltage ($V_{SSOLP(SS)}$) by soft-start operation charging current ($I_{SSOLP(SS)}$) sourced from the SS/OLP pin. Soft start is activated at power supply start-up by means of the SS/OLP pin voltage change from 0 V to 1.2 V. Timing is shown in Figure 7 and the next table.

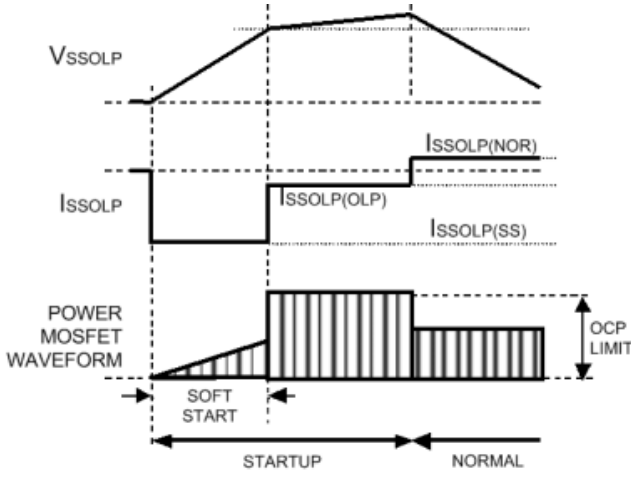

Figure 7 – Soft-start operation

By comparing the oscillation waveforms of the OLP pin and that of the internal control, soft start widening of the ON-width is activated. In addition, soft start is operated every time in the burst standby mode. Gradual increase of drain current suppresses magnetostriction noises from the transformer.

Soft-start timing (charging current: 550 mA)

C_{SS} (µF)	0.47	1	2.2	3.3	4.7
Time (ms)	1.0	2.2	4.8	7.2	10.3

NOTE: A large C_{SS} value also results in a longer time from OLP operation to latched mode.

Overload protection (OLP)

Figure 8 shows output characteristics of the secondary side when the OCP circuit is activated due to an overload at the secondary side output. When the output voltage drops in an overload mode, the bias winding voltage of the primary side drops proportionally, and the V_{CC} pin voltage drops below the 'operation-stop voltage' to deactivate the IC. Then, the circuit current decreases, and the V_{CC} pin voltage rises again by way of the start-up resistor (R2) charge current to reactivate the IC intermittently at the 'operation-start-up voltage'. However, where the transformer has multiple output windings and coupling is not good enough, the intermittent operation might not be sensed even if the output voltage drops in an overload mode, because the primary bias winding voltage would not drop. Although the intermittent operation is not realized, protection might still be by means of the OLP activation.

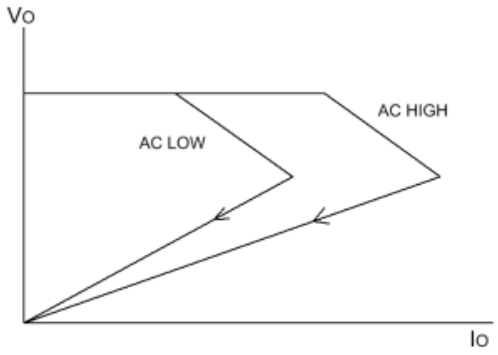

Figure 8 – Current-mode control

In the overload mode, where drain current is controlled by OCP operation, the secondary-side output voltage drops. Accordingly, the error-amplifier and photocoupler on the secondary side are cut off. The Series STR-W6750 regards the signal absence with continuous OCP operation as an overload status, and the SS/OLP pin voltage starts rising by $I_{SSOLP(OLP)}$ as shown in Figure 9. After the SS/OLP pin voltage keeps rising to 'OLP-Operation Threshold Voltage' ($V_{SSOLP(OLP)}$ = 4.9 V), the oscillation stops, and the IC goes into a latched mode.

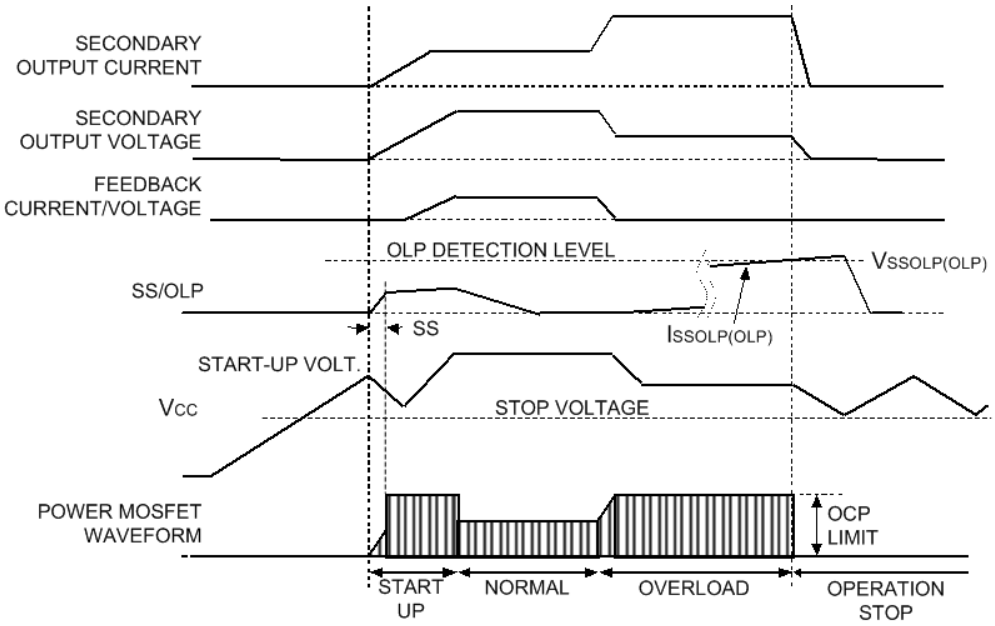

Figure 9 – Timing at overload

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036
SanKen

The time from OLP activation to a latched mode should be obtained from the following formula if $I_{SSOLP(OLP)}$ is from a constant-current circuit:

$$t = C_{SS} \times \Delta V / I_{SSOLP\ (OLP)}$$

where ΔV is the capacitor charging voltage of approximately 5 volts.

However, the $I_{SSOLP(OLP)}$ is voltage dependent on the SS/OLP pin voltage, and $I_{SSOLP(OLP)}$ drops as the SS/OLP pin voltage rises. The actual current value does not match the value calculated in the equation above. Therefore, actual load conditions should be carefully considered. Also, make sure that OCP operation at power supply start-up does NOT place the IC in a latched mode.

OLP timing (0~4.9 V, charging current: 11 mA)

C_{SS} (µF)	0.47	1.0	2.2	3.3	4.7
Time (ms)	209	445	980	1470	2094

During this period, if V_{CC} goes below the UVLO threshold voltage, the IC does not go into a latch mode, but goes into intermittent operation. Where the C_{SS} voltage rises to 4.9 V and V_{CC} does not go below the UVLO threshold voltage, the IC goes into a latched mode.

NOTE: A large C_{SS} value also results in a longer soft-start time.

Operation at power supply turn OFF

At power supply turn OFF, voltage on capacitor C_{SS}, which is externally connected to the SS/OLP pin, is discharged by way of an internal RESET circuit as shown in Figure 10. The RESET circuit does not operate in normal operation while the internal REG circuit operates.

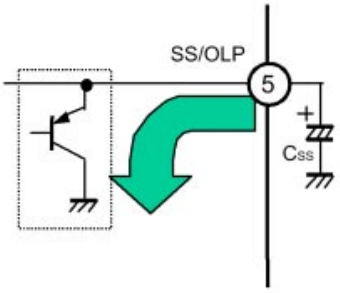

Figure 10 – Reset circuit at power turn OFF

How to deactivate the OLP circuit

To deactivate the OLP circuit while soft start is active, connect either a 47 kΩ resistor or a Zener diode to the SS/OLP pin (Figure 11). By doing this, OLP operation is deactivated at start-up or during an overload status.

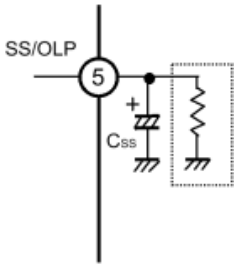

Figure 11 – OLP deactivation circuit

FB (Pin 6)

The FB pin is used in either a normal (constant-voltage-control circuit operation) or in the standby mode. Refer to Standby Operation (p8) for controlling in the standby mode.

REG circuit (or constant-voltage-control circuit)

Series STR-W6750 adopts the current-mode control circuit for a REG circuit, which ensures stability with a heavy load. The peak value of MOSFET drain current (at ON-time) is changed by comparing the FB pin voltage with the internal V_{OCPM}. OFF-time becomes quasi-resonant operation synchronized to the reset signal from a transformer. Where no reset signal is input from the transformer, it becomes fixed oscillation frequency (approximately 22 kHz) set by the internal oscillator circuit. The timing chart is shown in Figure 12, and the internal circuit diagram of the REG circuit is shown in Figure 13.

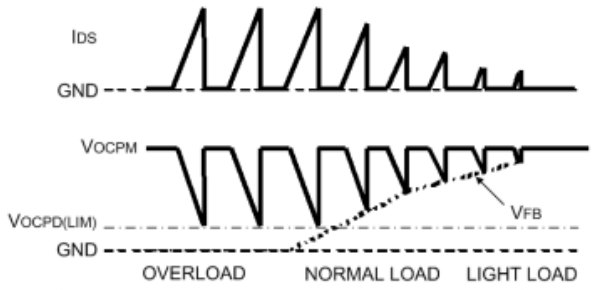

Figure 12 – Constant-voltage control (quasi-resonant signal ruled out)

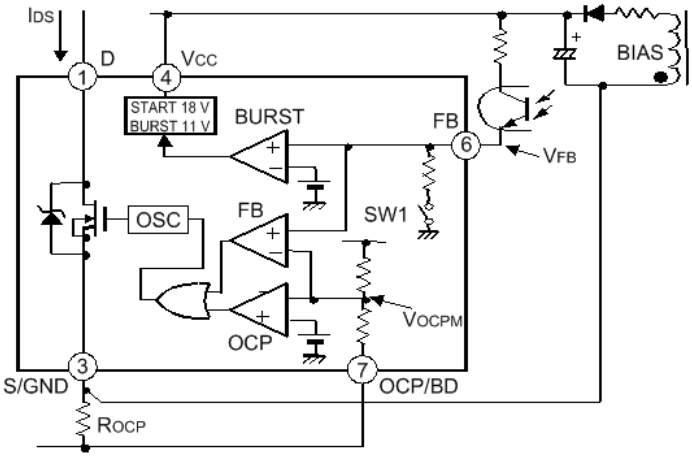

Figure 13 – REG functional block diagram

The constant-voltage-control circuit feeds a control signal (FB current) from an error amplifier into pin 6 by way of the isolating photocoupler. The input FB current is transformed into feedback voltage V_{FB} by the internal resistor (SW1 is ON during normal status). Voltage waveform (V_{OCPM}) from the drain current waveform is input to the inverting input terminal of the FB comparator.

Figure 12 shows the FB current is decreased to nearly zero in an overload, when the drain current is restricted to below the current value set by the overcurrent protection circuit.

In the period from normal load to light load in Figure 12, the drain current decreases because the FB current increases and V_{FB} rises. When V_{FB} exceeds the FB pin threshold voltage ($V_{FB(OFF)}$, 1.45 V) at light load, intermittent oscillation starts so as not to raise the secondary-side output voltage.

OCP/BD (Pin 7)

The OCP/BD pin functions as overcurrent detection, bottom-skip, and quasi-resonant-operation control. Refer to the next page for quasi-resonant and bottom-skip operation descriptions.

Negative-detection type OCP circuit

The OCP circuit of the Series STR-W6750 is a pulse-by-pulse type, which detects the peak value of the MOSFET drain current each pulse and inverts the oscillator output. As shown in Figure 14, the overcurrent sense resistor, R_{OCP}, is connected externally along with R4 and C5. R4 and C5 are to prevent malfunction caused by surges when the MOSFET switches ON. When the MOSFET switches ON, switching current occurs, and a voltage is developed across R_{OCP}. After that, the MOSFET turns OFF when the OCP/BD pin voltage reaches $V_{OCPBD(LIM)}$.

The threshold voltage of the OCP/BD pin, $V_{OCPBD(LIM)}$, is –0.94 V. The OCP circuit adopts negative-detection, which creates the detecting voltage, V_{OCPM}, in the control part by dividing the voltage (V_1 + V_{ROCP}) with RB1, RB2, and R4. Because RB1 and RB2 are resistors incorporated in the IC, taking variance of RB1 and RB2 (defined as I_{OCPBD} in the specifications) into consideration, the value of R4 should be small, between 100 Ω and 330 Ω. Select capacitor C5 (100 pF to 680 pF target value) for good thermal behavior. A high capacitance value results in slow response time, ending up with an increase in peak drain current during a transient and at start-up.

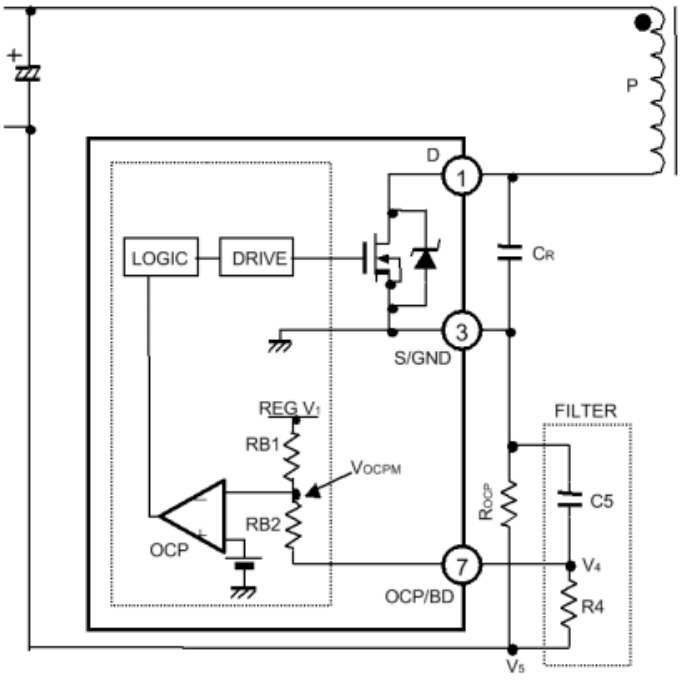

Figure 14 – OCP functional block diagram

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036
SanKen

OPERATION DESCRIPTIONS

Quasi-Resonant and Bottom-Skip Operation

Quasi-resonant operation

Quasi-resonant operation matches the timing of the MOSFET turn-ON to the bottom point of the voltage resonant waveform, namely, ½ cycle of the resonant frequency ($C_R \times L_P$), after the transformer discharges energy.

As shown in Figure 15, the voltage resonant capacitor, C_R, is connected between the drain and source, and the delay circuit, C10, D3, D4, and R9 are connected between the bias winding and the OCP/BD pin. When the MOSFET turns OFF, a quasi-resonant signal is generated from the fly-back voltage in the bias winding, and the BD comparator inside the IC operates, enabling quasi-resonant operation. Even after the energy of the transformer is discharged by way of the delay circuit, the quasi-resonant signal imposed on pin 7 does not drop immediately. This is because C10 is discharged by R4, and the voltage drops to the threshold voltage, $V_{OCPBD(TH1)}$, at 0.4 V after a certain period.

The delay time needs to be set by adjusting C10, monitoring the operating waveform, so that the MOSFET turns ON when the V_{DS} of the MOSFET hits the lowest point.

In addition to the quasi-resonant operation, the IC incorporates a 'bottom-skip operation' function in order to suppress the increase of oscillating frequency during a light-to-medium load. It lengthens the OFF-time in accordance with the load status. Change-over timing between the quasi-resonant and bottom-skip operation is described on page 8.

When the quasi-resonant signal voltage imposed on the OCP/BD pin is below $V_{OCPBD(TH2)}$ at 0.8 V, the IC goes into PWM operation with a fixed oscillating frequency of 22 kHz.

PWM operation is also activated at power supply start-up or at low bias winding voltage due to a winding short, which lowers oscillating frequency and reduces MOSFET stress. After the quasi-resonant signal exceeds $V_{OCPBD(TH2)}$ at 0.8 V, the MOSFET remains OFF during $V_{OCPBD(TH1)}$ at 0.4 V and higher. A voltage difference between $V_{OCPBD(TH1)}$ and $V_{OCPBD(TH2)}$ prevents malfunction.

In setting R9 and R4, the quasi-resonant signal imposed on the OCP/BD pin needs to be 5 V or less. In a normal condition, it should be approximately 1.5 V. The value of R4 is 100 Ω to 330 Ω and R_{OCP} is small enough to be ruled out. The bias winding output voltage is set at 18 V. To make the OCP/BD pin voltage 1.5 V or higher, R9 value is to be 1 kΩ to 3.3 kΩ.

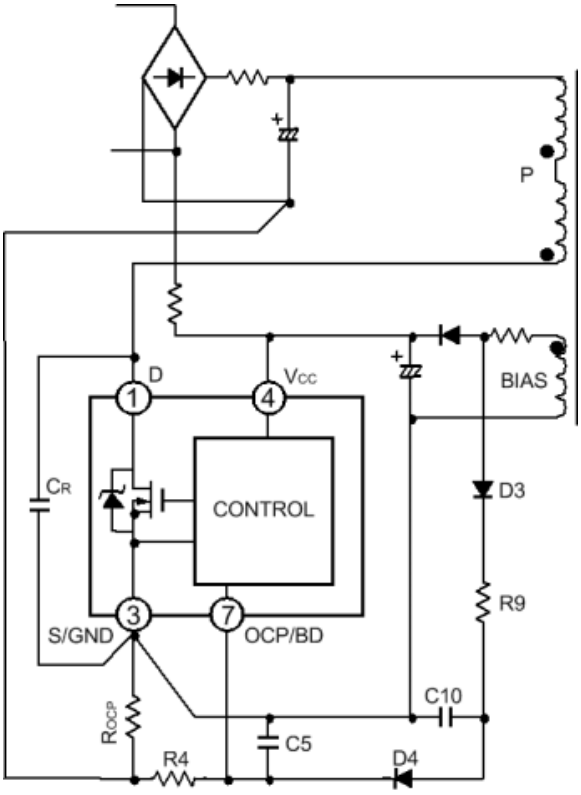

Figure 15 – Quasi-resonant and delay circuit

However, R9 needs to be considered together with C10 capacitance relative to setting up the delay time. R9 determines the time constant with C10 capacitance. Assuming the time constant is 2.2 ms, R4 is 220 Ω, R9 is 2.2 kΩ and C10 is 1000 pF, then proper selection should be done while looking at the quasi-resonant signal and V_{DS} waveform in the actual application.

Bottom-skip operation (shift from quasi-resonant operation)

The basic bottom-skip operation is activated at 'light load' by judging secondary load status by means of the drain current value (actually OCP/BD pin voltage). If the load status is judged 'heavy load', the IC goes into quasi-resonant operation. Judging is made by reading the OCP/BD pin voltage during the falling edge of the MOSFET gate voltage. Also, the quantity of falling edges (OCP/BD pin voltage is less than $V_{OCPBD(TH1)}$) of quasi-resonant signal is counted to be utilized to turn the MOSFET ON in accordance with the mode described above.

■ Quasi-resonant operation → bottom-skip operation

Quasi-resonance is operated under the absolute condition of V_{OCP} greater than $V_{OCPBD(BS2)}$. When the load becomes lighter and the drain current drops to make V_{OCP} less than $V_{OCPBD(BS2)}$, the operation is shifted to the bottom-skip mode, and the reference voltage is automatically changed to $V_{OCPBD(BS1)}$. Figure 16 shows shift timing from quasi-resonant operation to bottom-skip operation.

■ Bottom-skip operation → quasi-resonant operation

The bottom-skip is operated under the absolute condition of V_{OCP} less than $V_{OCPBD(BS2)}$. When the load becomes heavier and the drain current increases to make V_{OCP} greater than $V_{OCPBD(BS2)}$, the operation is shifted to the quasi-resonant mode, and the reference voltage is automatically changed to $V_{OCPBD(BS2)}$. V_{OCP} is the OCP/BD pin voltage at the falling edge of the MOSFET gate voltage.

As described above, the reference voltage for bottom-skip operation, $V_{OCPBD(BS1)}$ and $V_{OCPBD(BS2)}$, has hysteresis to make a stable operation shift as shown in Figure 17.

Standby Operation

The Series STR-W6750 devices incorporate the burst-mode function to reduce power consumption in the standby mode. Two modes are available. One is auto-burst mode, and the other (for lowest possible power dissipation) is externally triggered burst operation.

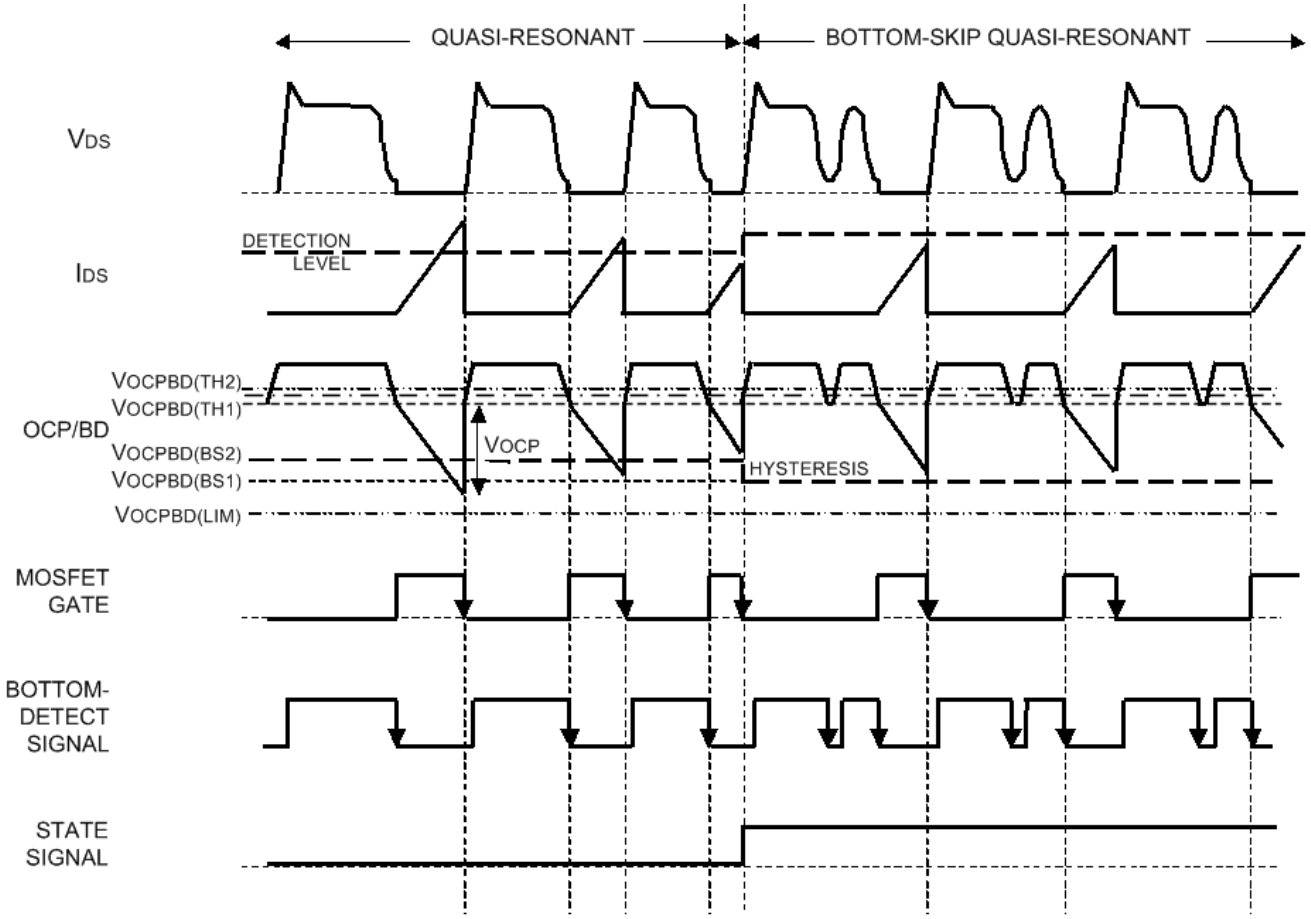

Figure 16 – Quasi-resonant to bottom-skip operation timing

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036
SanKen

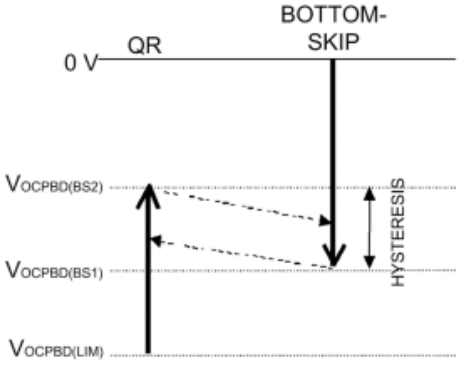

Figure 17 – Operation mode shift

Auto-burst mode

The standby mode is started by internally sensing the drain current pulse. Because the minimum drain pulse width is limited to the minimum ON-time pulse width of 1 µs, at light load the power supply can not lower its output power any more, and the output voltage starts increasing. When the FB pin voltage exceeds the FB standby operation threshold voltage $V_{FB(S)}$, the IC stops working until V_{FB} drops and then the power supply starts working again. This operation resembles burst-mode operation.

External trigger

Standby is also remotely controlled by a clamp on the secondary side to reduce the output voltage. Then, the transformer winding voltage drops and it reduces the bias winding voltage and the V_{CC} pin voltage (pin 4) decreases. When the V_{CC} pin voltage reaches the operation-stop voltage (9.7 V), the IC stops its operation, and current consumption of the IC becomes 'Circuit Current at Standby & Non-Operation', $I_{CC(S)}$. The IC will not restart its operation until the V_{CC} pin voltage rises to 'Operation Start-Up Voltage' by charging the start-up capacitor (C3) through the start-up resistor (R2). By repeating this cycle, the IC maintains the burst-mode. This is illustrated in Figure 18.

In order to eliminate the transformer's magnetostriction noises in the burst-mode, the voltage difference between the 'Standby Operation Start-Up Power Supply Voltage' and 'Operation-Stop Voltage' is designed to be small. By doing this, the operating frequency is increased without increasing the losses in the start-up resistor, and the IC is in a mode where switching current is reduced to as low a level as possible.

NOTE: During transitions between standby and nominal operation, because the STR-W6750 is not pumping energy, make sure that nominal output load is not applied, otherwise output voltage will drop significantly and will affect the entire system operation.

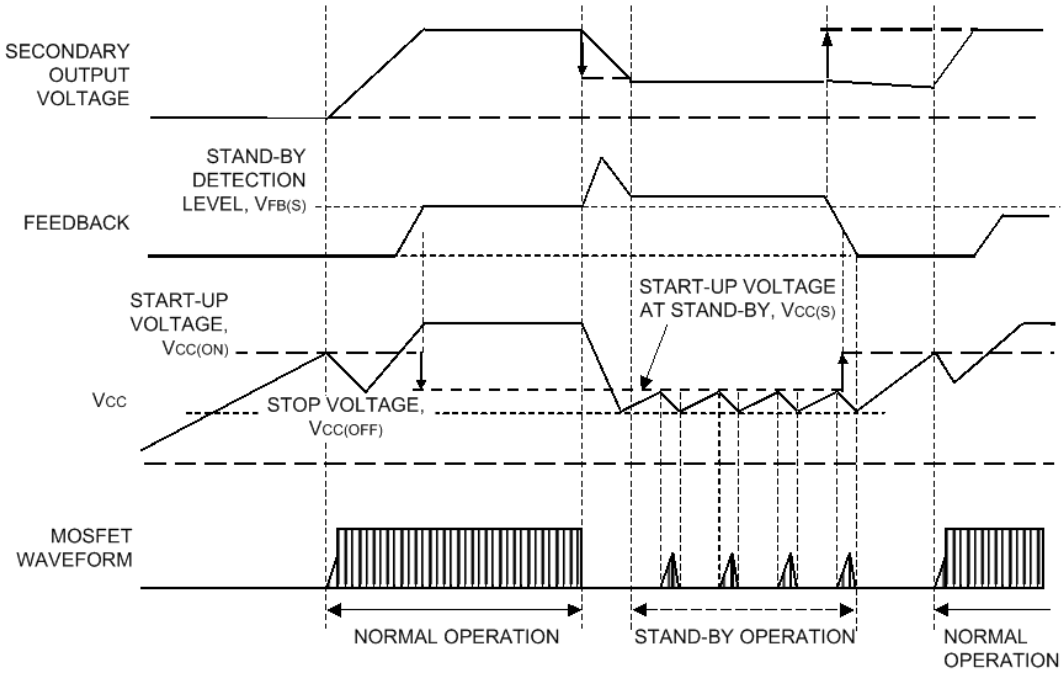

Figure 18 – Operation shift

Gate Step-Drive Circuit

The Series STR-W6750 incorporates a step-drive circuit (Figure 19) for driving the MOSFET, which reduces noise when the MOSFET turns ON. The drive current, when the MOSFET turns ON, is at first limited only by RG1, and the gate voltage is increased gradually, and then rapidly in approximately 0.9 µs via [RG1 + RG2]. Drive voltage then uses the constant-voltage drive circuit, maintained at V_{DRM} = 7.5 V, which is not affected by V_{CC}. The MOSFET gate charge is rapidly discharged through RG3 when the MOSFET turns OFF.

Maximum ON-Time Control Function

The MOSFET ON-time is limited during transients such as at low input voltage and at ON and OFF of ac input. The maximum ON-time is set at about 70% of the oscillation cycle ($1/f_{osc}$ = 45 µs), or approximately 32 µs. In designing a power supply, the MOSFET ON-time at maximum load and at minimum input voltage should be thoroughly considered.

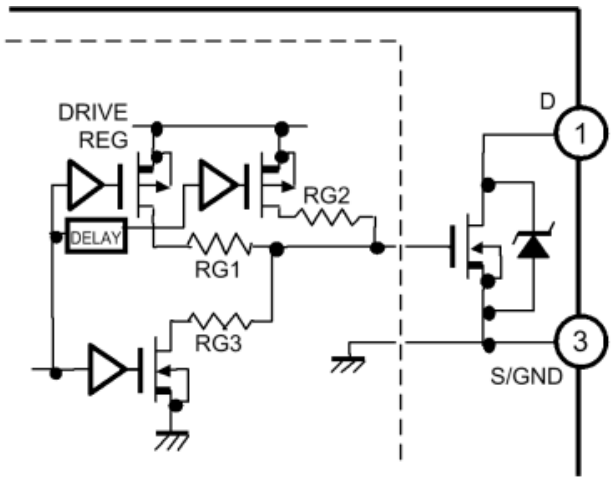

Figure 19 – Step drive circuit

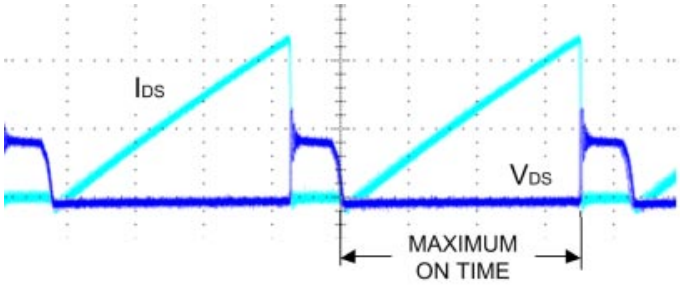

Figure 20 – Maximum ON-time

WARNING — These devices are designed to be operated at lethal voltages and energy levels. Circuit designs that embody these components must conform with applicable safety requirements. Precautions must be taken to prevent accidental contact with power-line potentials. Do not connect grounded test equipment.

The use of an isolation transformer is recommended during circuit development and breadboarding.

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036
SanKen

TRANSFORMER PARAMETERS

Basically, the same type of transformer as that for a conventional quasi-resonant circuit is recommended. The primary inductance, L_p, is determined by the following:

$$L_p = \frac{(V_{IN}\, D)^2}{\left(\frac{\sqrt{2\, P_O\, f_{osc}}}{\eta} + V_{IN}\, \pi\, f_{osc}\, D\, \sqrt{C_R}\right)^2}$$

where P_O = maximum output power,
f_{osc} = minimum oscillating frequency,
D = ON duty cycle at minimum $V_{IN(ac)}$,
η = transformer conversion efficiency (0.9 in the case of CTV, 0.75 to 0.85 in the case of low output voltage), and
V_{IN} = rectified and smoothed dc input voltage at minimum $V_{IN(ac)}$.

Turn-ON delay results in duty change in a quasi-resonant operation, therefore, duty correction is necessary. From the following, the number of turns, peak switching current (I_{dp}), corrected duty cycle (D´), delay time (t_d), and others can be obtained:

$$t_d = \pi \sqrt{L_p\, C_R}$$

$$D' = D\,(1 - [f_{osc}\, t_d])$$

$$I_{in} = P_O/(\eta^2\, V_{IN})$$

$$N_p = \sqrt{Lp/AL}$$

$$N_s = N_p\, (V_O + V_F)/(D\, V)$$

where I_{in} = average dc input current,
I_{dp} = peak switching current, and
C_R = voltage resonance capacitance.

In addition, in the design of the transformer, using 130% of the estimated peak switching current is recommended to estimate if the transformer saturates based on the curve of N × I-limit(AT) vs AL-value (nH/N^2).

Instead of performing the calculations above, software that provides a complete *Flyback Transformer Design Tool* is available.

TV application concerns:

- Rather than winding with a single thick wire, a thin and bifilar or trifilar winding across the entire width of bobbin is recommended.
- For windings where N_p and +B are a large number of turns, divisional sandwich winding is recommended.
- For an output where a tight regulation is required, winding with good coupling with S1 (+B) is recommended.
- For the +B winding, better coupling by use of litz wire is required. In case the litz wire does not fit into a bobbin's winding width, reduce the wire size, and use several of them in strands.
- For improved thermal design:

  Leakage flux of wires close to the core center becomes large. Eddy current can be reduced by the use of litz wire.

  In case the entire winding does not fit into available winding thickness, reduce the size of wires from outer side.

  Wire diameter is determined by actual current and should be less than 4 A/square mm.

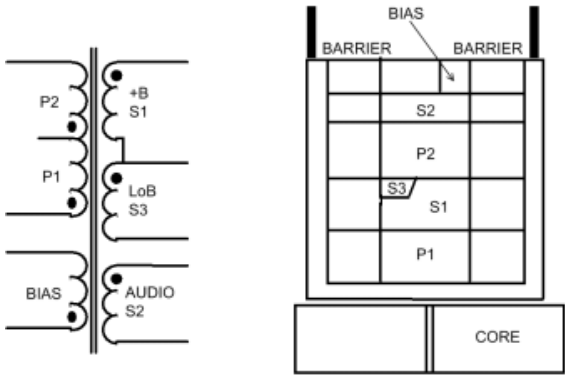

Figure 21 – Example of TV transformer

Single and/or low-voltage output concerns:

- Wind so that wires are parallel and with good coupling.
- Sandwich winding is recommended.

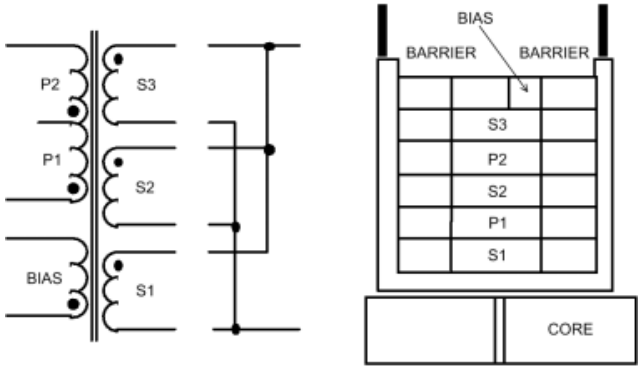

Figure 22 – Example of low-output voltage transformer

GENERAL CONSIDERATIONS

Universal AC Input Correction in OCP

With a universal ac input application, as described in Overload Protection (p4), the load conditions for OCP activation will vary according to input voltage level, 110 V or 230 V. Figure 23 illustrates a solution.

In the loop surrounded by the dashed line, the bias winding negative output is produced when sensing overcurrent by use of the principle that a voltage proportional to input voltage level is generated when the MOSFET switches ON.

The Zener diode is set to be ON with a 230 V ac input, but not to be activated with a 110 V ac input.

When the bias winding output voltage is 18 V, the resistor, Zener, and diode within the dashed line are recommended:

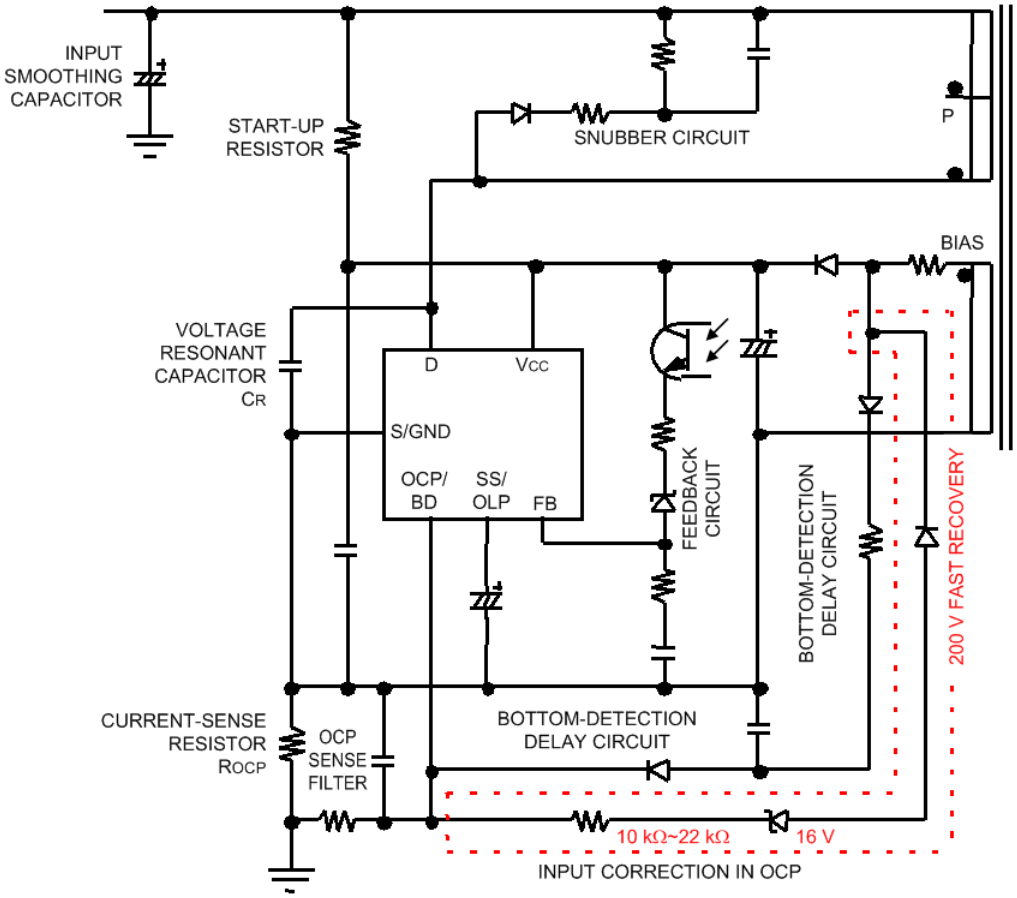

Figure 23 –
Universal ac input OCP

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036
SanKen

OCP on FB Pin

As was presented in Figure 23, in the feedback circuit portion, a Zener diode is connected in series with the photocoupler. This is a countermeasure against a FB-pin voltage rise over 9 V in the UVLO burst mode. The absolute maximum FB-pin voltage is 9 V, and a Zener diode voltage of 5.6 V to 6.2 V is recommended.

Output Regulation and Transformer Noise During Standby and Burst Modes

Figure 24 presents a simplified circuit of the secondary output and V_O isolation circuits.

After the output voltage is shifted over to a lower level, the IC goes into a UVLO burst mode on the primary side. In this mode, sufficient power is not obtained, and deep ripple output voltage is generated, resulting in audible noises from the transformer, a sharp drop of output voltage, and unsustainable regulation. A larger output smoothing capacitor reduces this issue.

Load in an actual UVLO burst mode ranges between tens of milliohms and 0.2 Ω at a maximum.

In regard to the noises from the transformer, contact a transformer manufacturer as a precaution against possible varnish dissolving and ferrite core attaching.

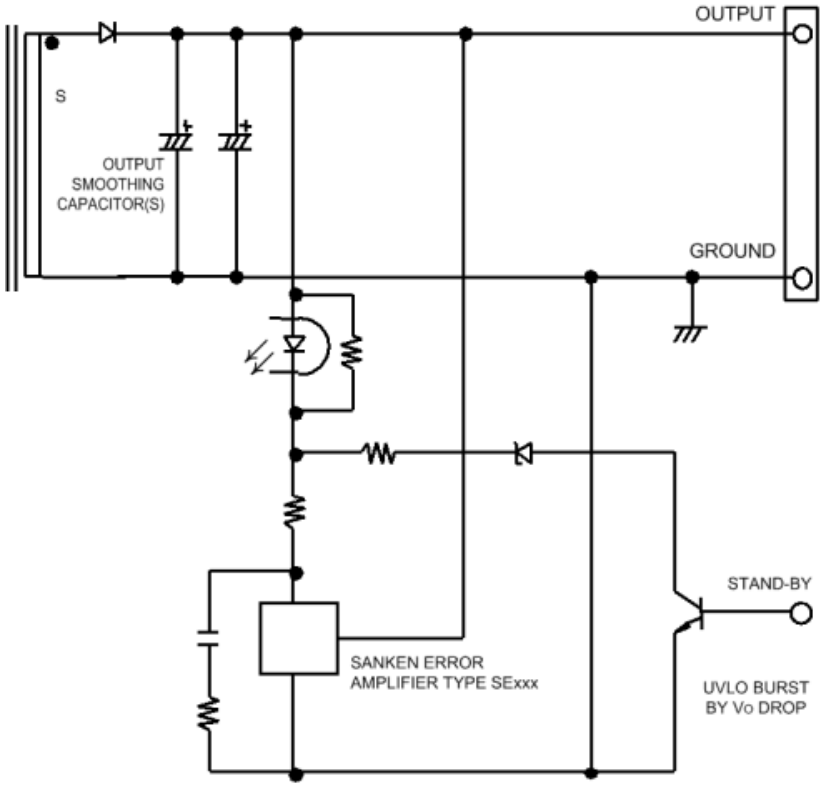

Figure 24 – Output circuit

DESIGN CONSIDERATIONS

Component Mount Considerations in SMPS Circuits

As pattern layout and component position may cause malfunctions of the IC, EMI noises, or power losses, the following guidelines should be followed;

■ Traces where high-frequency flow and high-current flow should be kept thick and short to lower line impedance.

■ The hatched area illustrated in Figure 25, where high frequencies and high currents create a loop, should be kept as small as possible.

■ S/GND and earth lines should be kept as thick and short as possible.

■ In off-line SMPS (switch-mode power supply) circuitry, because traces and paths of high voltage exist, component layout and trace length should be carefully considered, as required by safety standards.

■ Placement of power supply and heat-sinking designs should be carefully considered on the bench using an actual set.

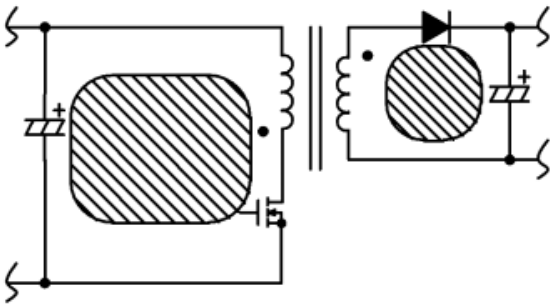

Figure 25 – High-frequency, high-current loops

Layout Considerations

■ In order to reduce or eliminate shared impedances, the S/GND pin (pin 3) and its peripheral components should be located as close together as possible as is illustrated in Figure 26. The trace from the overcurrent sense resistor to the input smoothing capacitor should be kept as short and thick as possible.

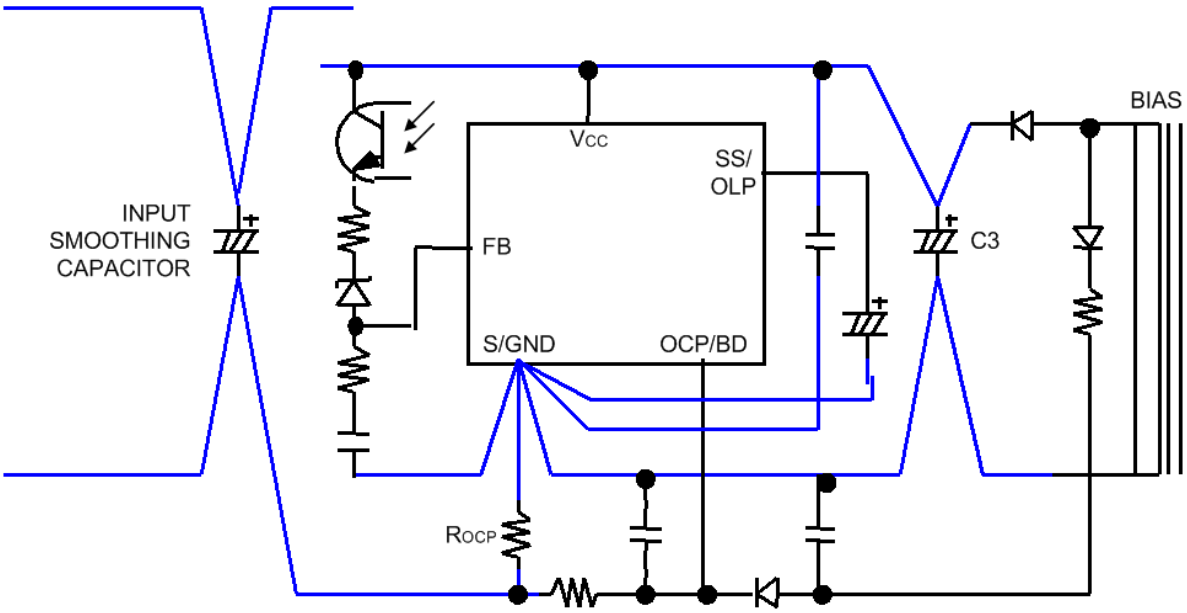

Figure 26 – Layout considerations

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036
SanKen

The products described herein are manufactured in Japan by Sanken Electric Co., Ltd. for sale by Allegro MicroSystems, Inc.

Sanken and Allegro reserve the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Therefore, the user is cautioned to verify that the information in this publication is current before placing any order.

When using the products described herein, the applicability and suitability of such products for the intended purpose shall be reviewed at the users responsibility.

Although Sanken undertakes to enhance the quality and reliability of its products, the occurrence of failure and defect of semiconductor products at a certain rate is inevitable.

Users of Sanken products are requested to take, at their own risk, preventative measures including safety design of the equipment or systems against any possible injury, death, fires or damages to society due to device failure or malfunction.

Sanken products listed in this publication are designed and intended for use as components in general-purpose electronic equipment or apparatus (home appliances, office equipment, telecommunication equipment, measuring equipment, etc.). Their use in any application requiring radiation hardness assurance (e.g., aerospace equipment) is not supported.

When considering the use of Sanken products in applications where higher reliability is required (transportation equipment and its control systems or equipment, fire- or burglar-alarm systems, various safety devices, etc.), contact a company sales representative to discuss and obtain written confirmation of your specifications.

The use of Sanken products without the written consent of Sanken in applications where extremely high reliability is required (aerospace equipment, nuclear power-control stations, life-support systems, etc.) is strictly prohibited.

The information included herein is believed to be accurate and reliable. Application and operation examples described in this publication are given for reference only and Sanken and Allegro assume no responsibility for any infringement of industrial property rights, intellectual property rights, or any other rights of Sanken or Allegro or any third party that may result from its use.